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Full Custom Physical Design of 4-Bit High Speed CSLA Using Grid Based Routing and Standard Cells

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Abstract: High speed addition and multiplication has always been a major requirement of high processing unit. The speed of addition and multiplication operations depends on speed of adders used in the design. Ripple carry adders (RCA) has better area utilization but has more delay, whereas the Carry Select Adder(CSLA) use two RCAs and increases the speed. The regular Carry Select Adder consists of dual ripple carry adders and multiplexers. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum of the next bit stages. The main disadvantage of regular CSLA is the large area due to multiple pairs of RCA and more power consumption. The modified CSLA using Common Boolean Logic (CBL) structure replaces the multiple use of RCA by using one inverter (INV) and OR gate. By using multiplexers, we can select the correct output result according to the logic state of carry-in signal from the previous bit stage. This structure consumes less area, delay and power. In this paper we have implemented two architectures of CSLA and simulated in cadence Spectre and compared the parameters like delay, area and power. The layout of CSLA using CBL logic is implemented using Cadence Layout editor-virtuoso with Standard cell library and grid routing techniques.

Keywords: Carry select adder, standard cell library, grid based routing.

I. INTRODUCTION

VLSI technology is a process that facilitates IC designers to combine many functions into a single chip which contains of billions of transistors and these ICs can be used for applications like microprocessor, memories, DSP. In VLSI technology, the main design constraints are area, power and speed. The main area of research in VLSI technology is optimization of area, power and delay. The performances of these processors usually depend on the arithmetic units used. The complex arithmetic operations can be easily decoded into simple elementary operations like addition and subtraction. Hence, the addition operation impacts the overall performance of a digital system like multipliers, DSP to execute algorithms like FIR, FFT etc. In this paper we have designed a standard cell based CSLA using CBL using cadence tools, where the area and power is reduced compared to other architectures of CSLA. The schematic is entered in composer-schematic studio and the circuit simulation and verification of the logic is done using cadence spectre. The customized layout of the proposed CSLA is implemented in cadence virtuoso tool and the DRC and LVS is cleared using cadence-Assura. The layout of the proposed adder is carried using self designed customized standard cell library, and the grid based routing is used in order to reduce area and errors in DRC and LVS.

II. SYSTEM ARCHITECTURE

The carry-select adder generally consists of two row of ripple carry adder to generate partial sum and carry and multiplexer is used to select the output. The first adder assumes the carry input as 1 and the other assumes carry

as 0. After the two partial results are calculated, the correct sum and carry is selected by mux. In this paper we have designed schematic of CSLA using RCA and CBL in cadence composer schematic.

A. CSLA using RCA

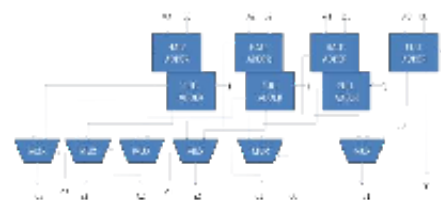


Fig.2.1: Regular CSLA using RCA

Fig.2.1 shows the basic building block of a carry-select adder, where the block size is 4-bit. It has dual ripple carry adder with 2:1 mux. The main disadvantage of this adder is large area due to multiple pairs of ripple carry adders and it can be also seen in the table 2.1 that mosfet count is 192 for this architecture. Since one ripple carry adder assumes a carry-in of 0 so we have used half adder, and the other assumes a carry-in of 1, by selecting the correct adder output from previous carry. Here the delay is reduced in compared to ripple carry adder. The carry output from the first block is given to the mux, if the carry out is logic zero then outputs from the half adder is selected, if the carry output is logic one then outputs from the full adder is selected.

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